Pierce-gate oscillator crystal load calculation

By Ramon Cerda

The Pierce-gate oscillator of Figure 1 is well recognized by most designers, but few understand how to specify the crystal correctly. The crystal used in the topology of Figure 1 can be either a fundamental AT-CUT or BT-CUT. A BT-CUT crystal has poor frequency stability over temperature compared to an AT-CUT. This topology uses a *parallel* crystal and not a *series* crystal. When a parallel crystal is specified, the crystal manufacturer will also require that you specify a *load capacitance*.

To understand load capacitance, think of a series LC circuit where the crystal is the *L* and the load capacitance is the *C*. The resonance frequency of the LC circuit will vary as a function of *L* and *C*. But in the crystal case, the *L* is fixed (temperature not being a parameter).

The parameter on the crystal data sheet that is controlled by the load capacitance is the tolerance or calibration of the center frequency at 25°C. If the oscillator circuit is not designed to match the load capacitance value, then the center frequency will not be within the tolerance limits of the data sheet. Interestingly enough, a so-called *parallel crystal* requires its capacitive load effectively be in series with its terminals.

So what load is your Pierce-gate oscillator presenting to the crystal? A simple calculation illustrated with Figure 2 will tell you.

C_{load} = {[C_{in}+C_1][$C2$+C_{out}]/[C_{in}+C_1+C_2+C_{out}]} + pcb strays (2~3pF)

Example: Let C_{in} = C_{out} = 5pF;
C_1 = C_2 = 20pF
Therefore, C_{load} = {[25][25]/[25+25]} + 3
= 12.5 + 3 = 15.5pF

Select C_{load} = 16pF

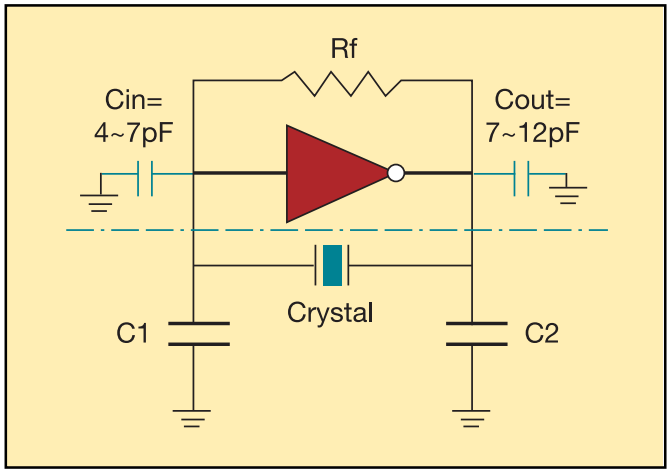

Figure 1. Pierce-gate oscillator diagram

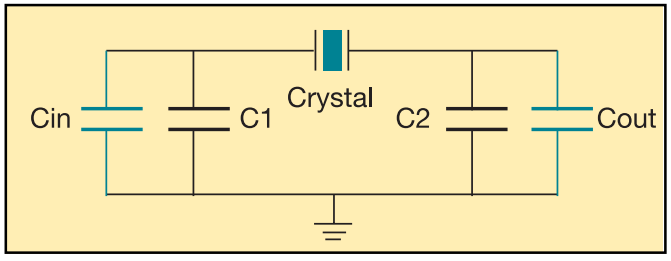

Figure 2. Calculating crystal's load capacitance.

The most important fact in Figure 2 that most designers neglect is the internal input and output capacitance of the inverter gate. These are significant in value compared to the external (C_1 and C_2). If C_{in} and C_{out} are not specified, then a guess value of 5 pF for each is a good start. The circuit can be later optimized by changing the starting values of C_1 and C_2. So don't throw away your major tolerance; calculate your oscillator capacitive load.

Now that you know how to calculate the load capacitance the circuit presents to the crystal, what load capacitance should you choose? Before answering this question, you need to know the sensitivity of the crystal center frequency vs. load capacitance. This is known as the trim sensitivity *S* and is given by:

$$S = -\frac{C_m}{2(C_o + C_{load})^2} \cdot 10^{-6} \text{ in ppm/pF}$$

where C_m is the motional capacitance of the crystal,
C_o is the shunt capacitance of the crystal,
and C_{load} is the load capacitance.

From the trim sensitivity equation you can see that the smaller you make C_{load}, the larger the trim sensitivity. In other words, if you are designing a fixed frequency clock, then you choose a high C_{load} value like 20 pF. However, if you are designing a variable frequency oscillator (VCXO), choose a low C_{load} value such as 14 pF.

The C_1 and C_2 values also affect the gain of the oscillator. The lower the values, higher the gain. Likewise, C_2/C_1 ratio also affects gain. To increase the gain, make C_1 smaller than C_2. RFD

ABOUT THE AUTHOR

Ramon Cerda is director of engineering at Crystek Crystals Corp., Fort Myers, Fla. He can be reached at rcerda@crystek.com