

Features

1.800 GHz - 1.860 GHz Range in Bands

Standard 3 Wire Interface

Small layout 0.582" × 0.8"



Applications

Digital Radio Equipment

Fixed Wireless Access

Satellite Communications Systems

Base Stations

Personal Communications Systems

Portable Radios

Test Instruments

Wireless Infrastructure

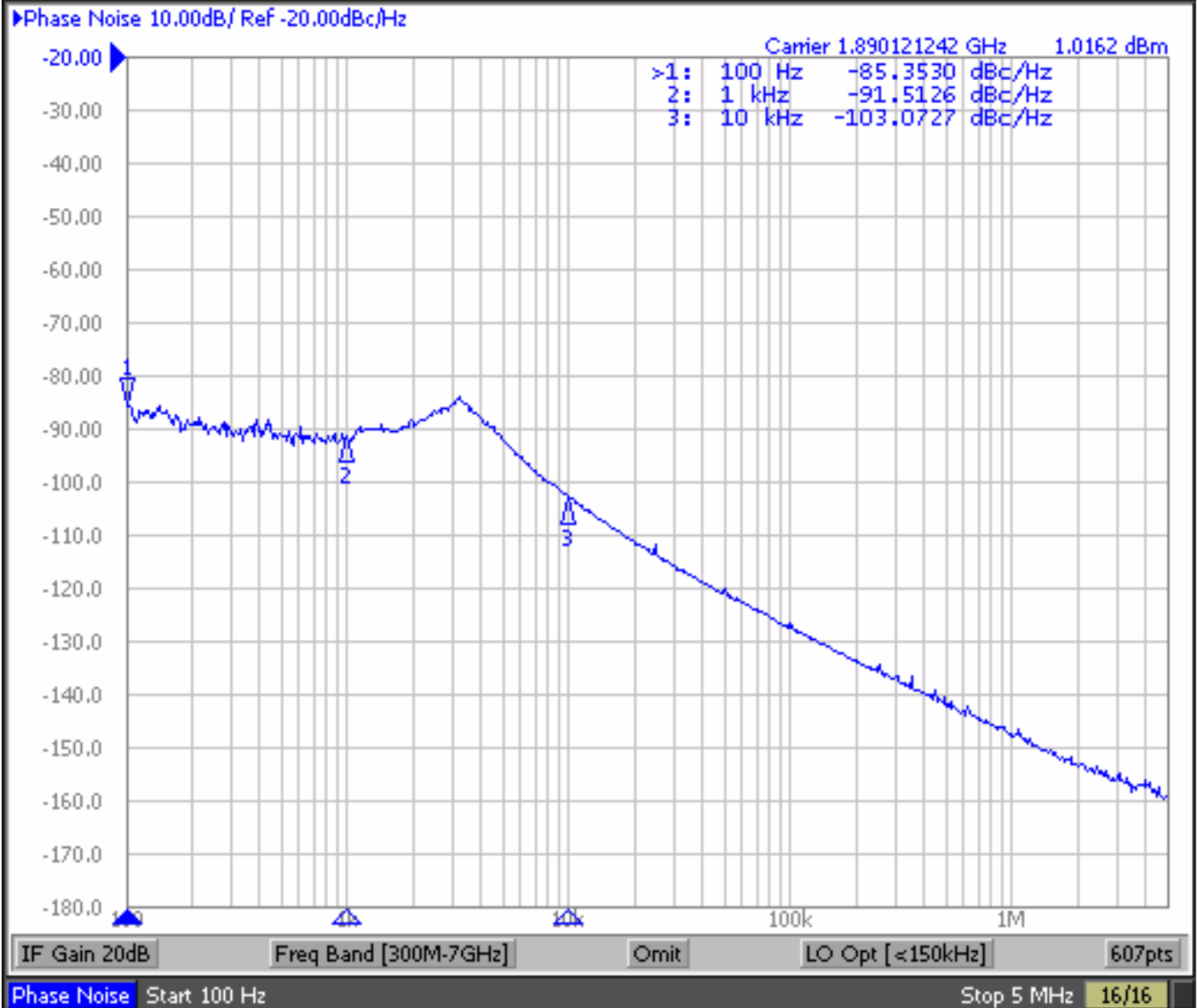
The CPLL58 is a complete PLL/Synthesizer needing only an external frequency reference and supply voltages for the internal PLL (phase lock loop) and VCO (voltage controlled oscillator). The Crystek CPLL58 is programmed using a standard three line interface (Data, Clock and Load Enable).

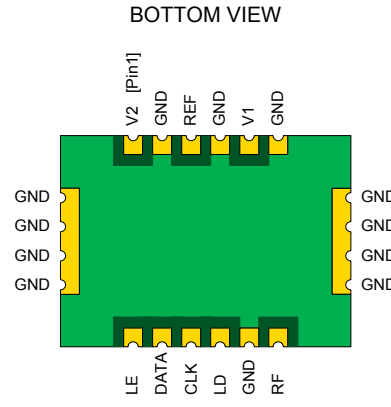
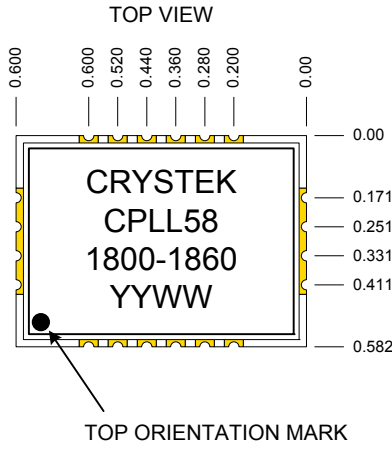
The CPLL58 family has been initially released to cover 1 GHz to 5 GHz in bands. It is housed in a compact 0.582-in. × 0.8-in. × 0.15-in. SMD package which saves board space. Typical phase noise at 4 GHz is -90 dBc/Hz at 10 kHz offset with 0 dBm minimum output power.



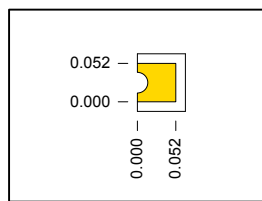
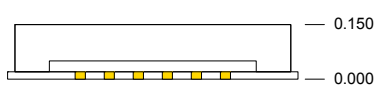
PERFORMANCE SPECIFICATION	MIN	TYP	MAX	UNITS
Frequency Range:	1.800		1.860	GHz
Step Size:		10		kHz
Settling Time, to within ± 1kHz (Freq. step < 25MHz):		1		msec
Output Power:	0	+3.0	+6.0	dBm
Output Phase Noise: (See Plot Below)				
@1kHz offset		-82	-80	dBc/Hz
@10kHz offset		-103	-98	dBc/Hz
@100kHz offset		-127	-122	dBc/Hz
@1MHz offset		-147	-142	dBc/Hz
Power Supply:				
V1=VCO Supply	4.75	5.0	5.25	Volts
V2=PLL Supply	2.7	3.0	3.3	Volts
Supply Current:				
I1=VCO Input Current		20		mA
I2=PLL Input Current		15		mA
Reference Feedthru		-80	-70	dBc
Harmonic Suppression (2nd Harmonic):				
2 nd		-20	-15	dBc
Reference Frequency		10		MHz
Input Reference Level	0.8		V2	Vp-p
Input Impedance		100k		Ohm
RF Output Impedance		50		Ohm
Operating Temperature Range:	-40		+85	°C
Logic Inputs (Clock, Data, and LE):				
Input "High" Voltage	1.4			
Input "Low" Voltage			0.6	Volts
Locked Detector (LD):				
Locked	1.4			Volts
Un-Locked			0.4	Volts

Agilent E5052A Signal Source Analyzer



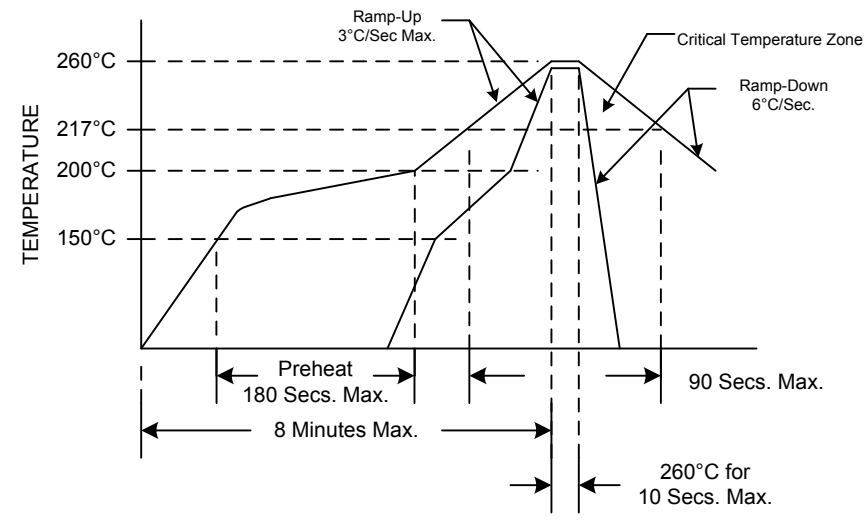


- LE = Load Enable, CMOS Input
- DATA = Serial Data Input
- CLK = Clock
- LD = Lock Detect
- REF = Reference Input
- V1 = Analog Supply Input (VCO)
- V2 = Digital Supply Input (PLL)
- RF = RF Output



Pad Detail

RECOMMENDED REFLOW SOLDERING PROFILE



ENVIRONMENTAL COMPLIANCE

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016

Timing Characteristics for CPLL58-1800-1860

Parameter ¹	Limit at T _{MIN} to T _{MAX} (B Version)	Unit	Test Conditions/Comments
t ₁	20	ns min	LE setup time
t ₂	10	ns min	DATA to CLOCK setup time
t ₃	10	ns min	DATA to CLOCK hold time
t ₄	25	ns min	CLOCK high duration
t ₅	25	ns min	CLOCK low duration
t ₆	10	ns min	CLOCK to LE setup time
t ₇	20	ns min	LE pulse width

¹Guaranteed by design, but not production tested.

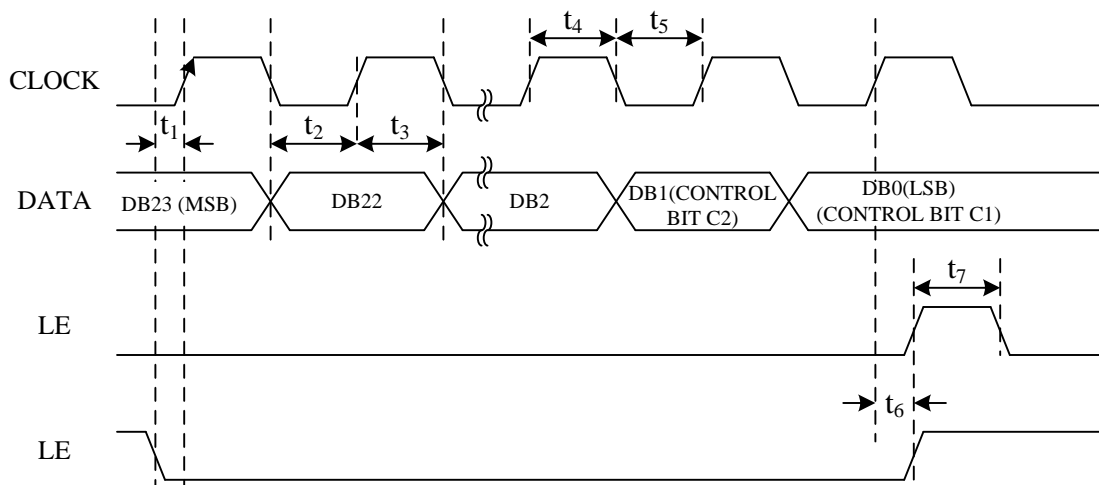
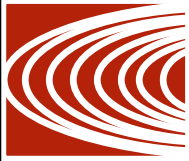


Figure 1. Timing Diagram



Register Summary

N-DIVIDER REG

FAST-LOCK	9-BIT RF N VALUE										12-BIT RF FRAC VALUE										CONTROL BITS		
	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1
FL1	N9	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C2(0)	C1(0)

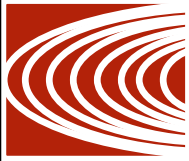
LOAD CONTROL	MUXOUT				RESERVED	PRESCALER	4-BIT R VALUE				12-BIT INTERPOLATOR MODULUS VALUE/FAST-LOCK TIMER										CONTROL BITS		
	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1
P3	M3	M2	M1	P2	P1	R4	R3	R2	R1	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C2(0)	C1(1)

RESERVED				REF _N DOUBLER	CP/2	CHARGE PUMP CURRENT SETTING				PHASE DETECTOR POLARITY	LOCK DETECT PRECISION	RF POWER-DOWN	RF CHARGE PUMP THREE-STATE	RF COUNTER RESET	CONTROL BITS	
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	U6	CP3	CP2	CP1	CP0	U5	U4	U3	U2	U1	C2(1)	C1(0)	

RESERVED	NOISE AND SPUR MODE					RESERVED			NOISE AND SPUR MODE	CONTROL BITS	
DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
T9	T8	T7	T6	T5	T4	T3	T2	T1	C2(1)	C1(1)	

Specifications subject to change without notice.





N-Divider Register Map

FAST-LOCK	9-BIT RF N VALUE (INT)										12-BIT FRAC VALUE (FRAC)										CONTROL BITS			
	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	FL1	N9	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C2(0)	C1(0)

F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	FRACTIONAL VALUE (FRAC)
0	0	0	0	0	0			0	0	0	0
0	0	0	0	0	1			0	0	1	1
0	0	0	0	1	0			0	1	0	2
0	0	0	0	1	1			0	1	1	3
.
.
1	1	1	1	0	0			1	0	0	4092
1	1	1	1	0	1			1	0	1	4093
1	1	1	1	1	0			1	1	0	4094
1	1	1	1	1	1			1	1	1	4095

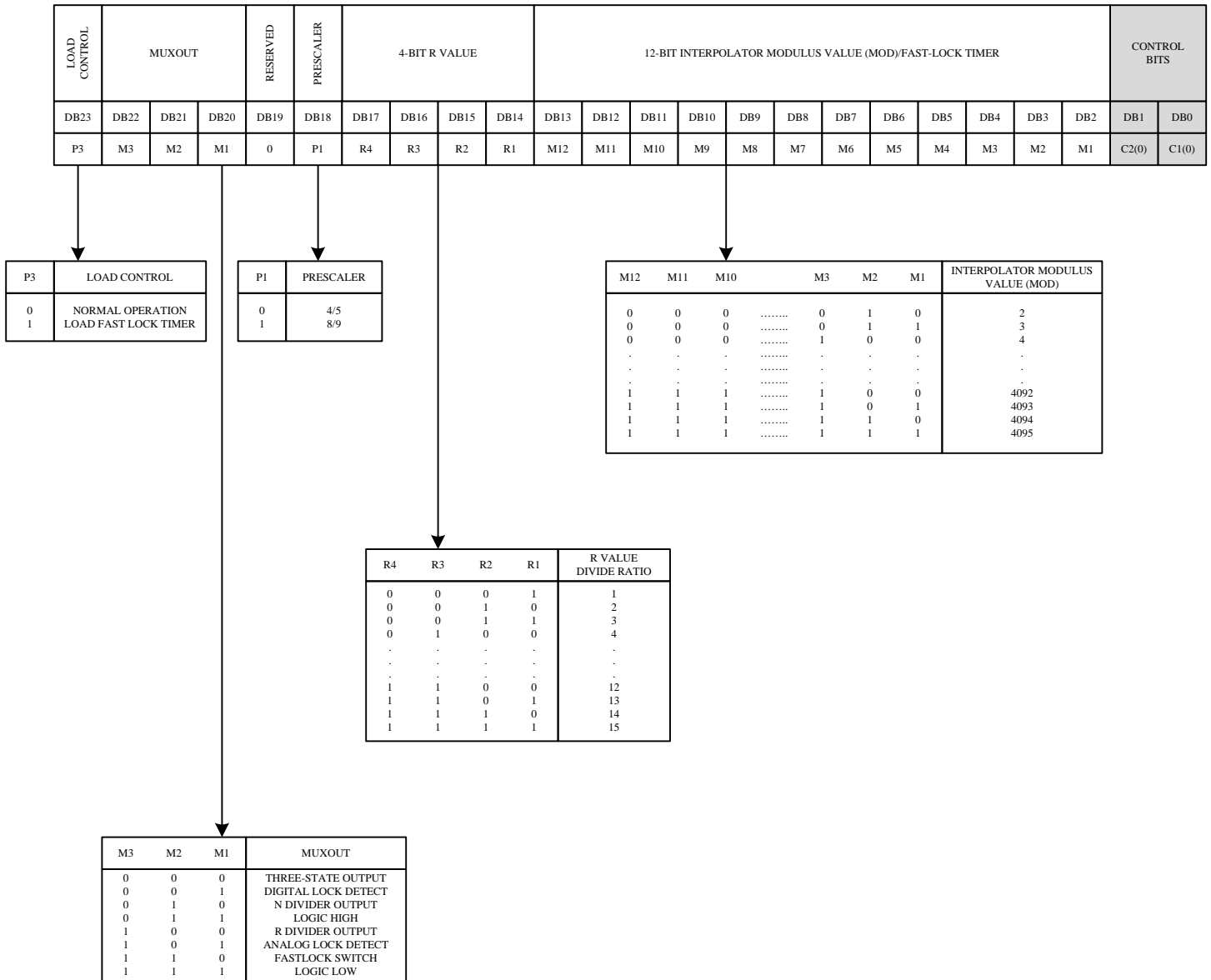
N9	N8	N7	N6	N5	N4	N3	N2	N1	INTERGER VALUE (INT)
0	0	0	0	1	1	1	1	0	31
0	0	0	1	0	0	0	0	1	32
0	0	0	1	0	0	0	1	0	33
0	0	0	1	0	0	0	1	1	34
.
.
1	1	1	1	1	1	1	0	1	509
1	1	1	1	1	1	1	1	0	510
1	1	1	1	1	1	1	1	1	511

FL1	FAST-LOCK
0	NORMAL OPERATION
1	FAST-LOCK ENABLED

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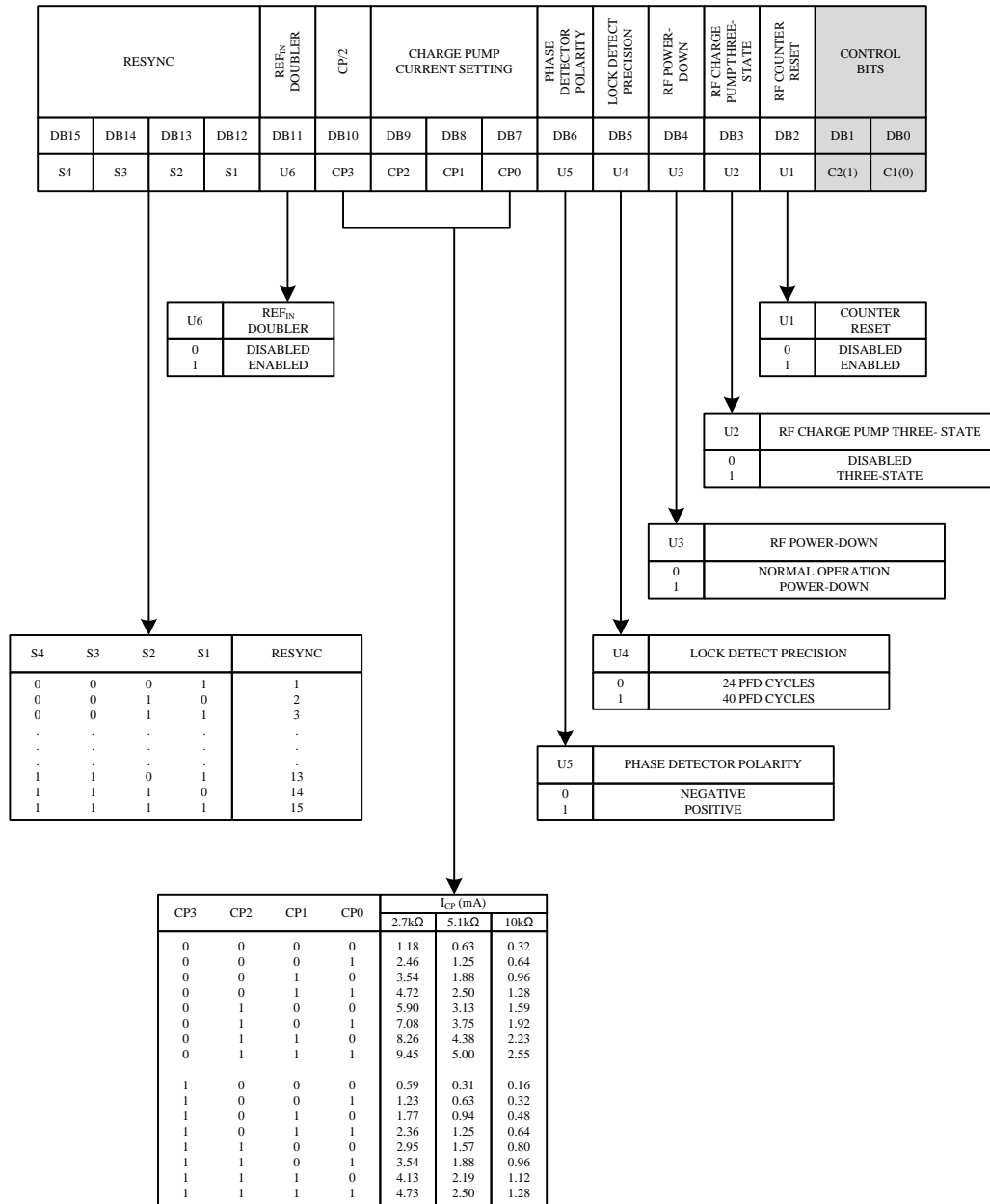


R-Divider Register Map

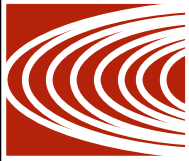


Specifications subject to change without notice.

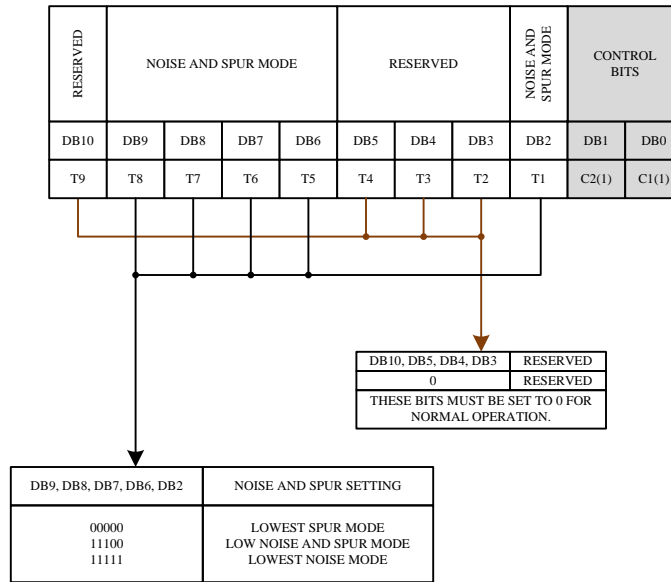
Control Register Map



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Noise and Spur Register



Programming Crystek p/n: CPLL58-1800-1860

TBD

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