

CCLD-575 Model
5×7.5 mm SMD, 3.3V, LVDS

CCLD-575 5×7.5mm SMD Ultra-Low Phase Noise LVDS Clock Oscillator



Model CCLD-575 has an industry leading phase noise for an LVDS oscillator. The noise floor is typically @ -160 dBc/Hz! This is at least 15 dB lower phase noise than most LVDS oscillators on the market today. Close-in phase noise is also excellent @ -90 dBc/Hz for the 100 MHz variant.

High Q Third Overtone crystal design provides ultra-low phase noise and very low jitter.



5×7.5mm SMD



Applications:

**Digital Video
SONET/SDH/DWDM
Storage Area Networks
Broadband Access
Ethernet, Gigabit Ethernet**

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Frequency Range:	50.000 MHz to 156.250 MHz*	<table border="1"> <thead> <tr> <th>*Standard Frequencies (MHz)</th> </tr> </thead> <tbody> <tr> <td>80.000</td> </tr> <tr> <td>100.000</td> </tr> <tr> <td>122.880</td> </tr> <tr> <td>125.000</td> </tr> <tr> <td>156.250</td> </tr> </tbody> </table>	*Standard Frequencies (MHz)	80.000	100.000	122.880	125.000	156.250
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122.880								
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156.250								
Frequency Stability Options:	±20ppm, ±25ppm, ±50ppm							
Operating Temperature Range:	-40°C to +85°C							
Storage Temperature Range:	-45°C to 90°C							
Input Voltage:	3.3V ± 0.3V							
Input Current:	66mA Max							
Output:	Differential LVDS							
Symmetry:	40/60% Max @ zero crossing point							
Rise/Fall Time:	250 ps Max (20% to 80%)							
Load:	100 ohms connected between OUT and COUT							
Output Low Voltage:	“0”=0.90 Min, 1.10 Max							
Output High Voltage:	“1”=1.43 Min, 1.60 Max							
Disable Time:	0.5 µs Max							
Enable Time:	4.0 µs Max							
Sub-harmonics:	None							
Aging:	<3ppm 1st year, <1ppm every year thereafter							

Part Number Example: CCLD-575X-25-100.000 3.3V, -40/85°C, ±25ppm, 100.000 MHz

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Ultra-Low Phase Noise

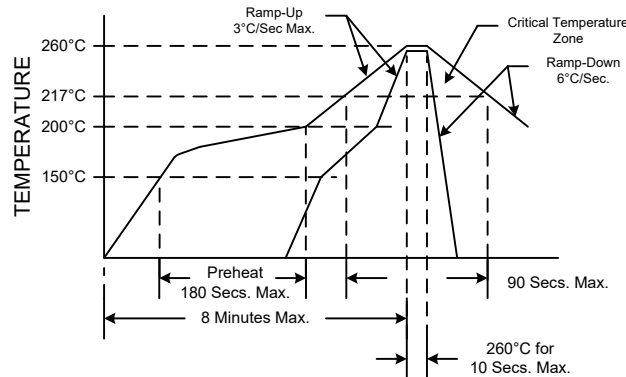
LVDS Clock Oscillator

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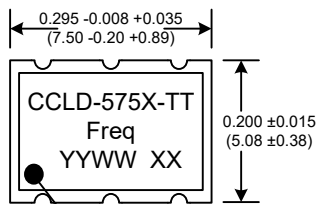


Mechanical:	
Shock:	MIL-STD-883, Method 2002, Condition B
Solderability:	MIL-STD-883, Method 2003
Vibration:	MIL-STD-883, Method 2007, Condition A
Solvent Resistance:	MIL-STD-202, Method 215
Resistance to Soldering Heat:	MIL-STD-202, Method 210, Condition I or J
Environmental:	
Thermal Shock:	MIL-STD-883, Method 1011, Condition A
Moisture Resistance:	MIL-STD-883, Method 1004

RECOMMENDED REFLOW SOLDERING PROFILE



NOTE: Reflow Profile with 240°C peak also acceptable.



Denotes pad 1

TT=Tolerance YYWW=Date Code XX=Lot Code

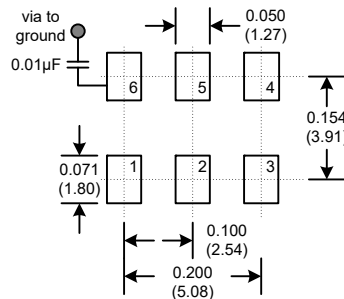
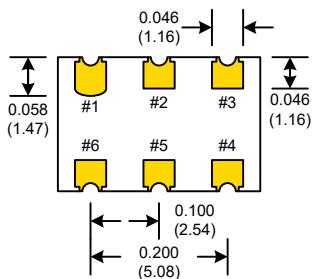
Dimensions inches (mm)

All dimensions are Max unless otherwise specified.



Enable/Disable	
Function pin 1	Output pin
Open or N/C "1" level 2.0V Min "0" level 0.8V Max	Active Active High Z

SUGGESTED PAD LAYOUT



PIN	Connection
1	Enable/Disable
2	N/C
3	GND
4	Output
5	Comp Output
6	Vcc

PAD FINISH: Immersion Gold (ENIG); 5 micro inches maximum

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