

## CVPD-970 Model

9×14 mm SMD, 3.3V, LVPECL

<b>Frequency Range:</b>	622.080 MHz to 670 MHz
<b>Frequency Stability:</b>	±25ppm
<b>Temperature Range:</b>	0°C to 70°C
(Option X)	-40°C to 85°C
<b>Storage:</b>	-45°C to 90°C
<b>Input Voltage:</b>	3.3V ±0.3V
<b>Control Voltage:</b>	1.65V ±1.65V
<b>Input Current:</b>	80mA Max
<b>Output:</b>	Differential LVPECL
Symmetry:	49/51% Typical, 45/55% Max @ zero crossing point
Rise/Fall Time:	0.4ns Max (20% to 80%)
Pullability APR:	±50ppm Min
Linearity:	±10% Max
Load:	Terminated to Vdd-2V into 50 ohms
Logic "1" Level:	Vcc-0.96V Min, Vcc-0.81V Max
Logic "0" Level:	Vcc-1.85V Min, Vcc-1.65V Max
Disable Time:	100ns Max
Start-up Time:	2ms Typical, 10ms Max
<b>Modulation BW:</b>	>10kHz @ -3dB
<b>Sub-harmonics:</b>	-40dBc
<b>Period Jitter:</b> (20,000 periods)	<5ps RMS (1-sigma) Max
<b>Phase Jitter:</b> 12kHz~20MHz	<1ps RMS (1-sigma) Max
50kHz~80MHz	<1ps RMS (1-sigma) Max
<b>Phase Noise Typical:</b> 100Hz	-80 dBc/Hz
1kHz	-108 dBc/Hz
10kHz	-132 dBc/Hz
100kHz	-140 dBc/Hz
<b>Aging:</b>	<3ppm 1 <sup>st</sup> year, <2ppm every year thereafter



### Applications:

10 Gigabit Ethernet  
OC48: Forward Error Correction  
Broadband Networks  
SONET/SDH/DWD  
ATM  
Network/switch  
Telecom

Designed using FR5 PCB & HFF crystal technology to provide a Low Noise, Low Jitter Voltage Controlled Clock Oscillator solution at a competitive price.



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# Differential LVPECL VCXO



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### Crystek Part Number Guide

CVPD - 970 - X - 622.080

#1 #2 #3 #4

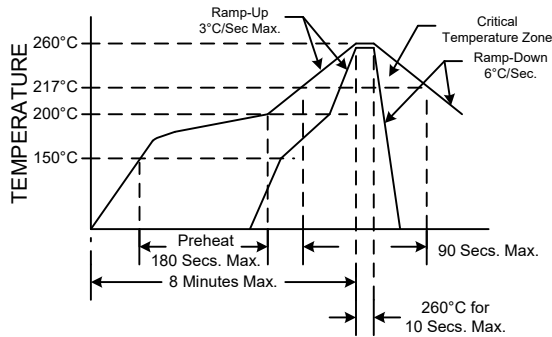
- #1 Crystek 9x14 SMD PECL VCXO
- #2 Model 970 = High Frequency 3.3V
- #3 Temp. Range: Blank = 0/70°C, X = -40/85°C
- #4 Frequency in MHz: 3 or 6 decimal places

Example:  
CVPD-970X-622.080 = 3.3V, -40/85°C, 622.080 MHz

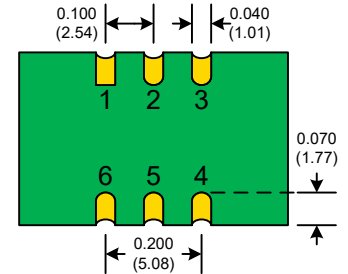
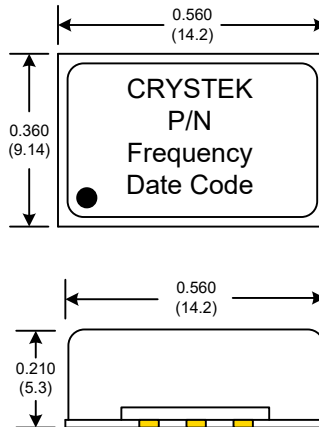
### Standard Frequencies MHz

622.080	666.514300
625.000	669.128100
644.531300	669.326500

### RECOMMENDED REFLOW SOLDERING PROFILE



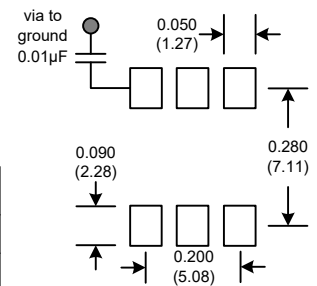
NOTE: Reflow Profile with 240°C peak also acceptable.



**PAD FINISH:** Immersion Gold (ENIG); 5 micro inches maximum

PIN	Function
1	Vcont
2	E/D
3	GND
4	OUT
5	COU
6	Vdd

### SUGGESTED PAD LAYOUT



Enable/Disable Function	
Pin 2	Output pin
Open	Active
"0" level Vcc-1.620V Max	Active
"1" level Vcc-1.025V Min	Disabled
Disabled State: Pin 4 will assume a fixed level of logic "0" Pin 5 will assume a fixed level of logic "1"	

### Mechanical:

Shock:  
Solderability:  
Vibration:  
Solvent Resistance:  
Resistance to Soldering Heat:

MIL-STD-883, Method 2002, Condition B  
MIL-STD-883, Method 2003  
MIL-STD-883, Method 2007, Condition A  
MIL-STD-202, Method 215  
MIL-STD-202, Method 210, Condition I or J

### Environmental:

Thermal Shock:  
Moisture Resistance:

MIL-STD-883, Method 1011, Condition A  
MIL-STD-883, Method 1004

### Packaging:

Tape/Reel:

100ea, 250ea, 500ea 24mm Tape

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